High mobility and high on/off ratio field-effect transistors based on chemical vapor deposited single-crystal MoS2 grains

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We report the electrical characteristics of field-effect transistors (FETs) with single-crystal molybdenum disulfide (MoS2) channels synthesized by chemical vapor deposition (CVD). For a bilayer MoS2 FET, the field-effect mobility is \(\sim 17 \text{cm}^2\text{V}^{-1}\text{s}^{-1}\) and the on/off current ratio is \(\sim 10^6\), which are much higher than those of FETs based on CVD polycrystalline MoS2 films. By avoiding the detrimental effects of the grain boundaries and the contamination introduced by the transfer process, the quality of the CVD MoS2 atomic layers deposited directly on SiO2 is comparable to or better than the exfoliated MoS2 flakes. The result shows that CVD is a viable method to synthesize high quality MoS2 atomic layers. © 2013 AIP Publishing LLC [http://dx.doi.org/10.1063/1.4801861]

The single-layer (SL) graphene has a linear Dirac-like band structure with no bandgap, which leads to the formation of massless Dirac fermions with remarkable electronic properties, e.g., an effective speed of light \(v_F\approx 10^6 \text{ms}^{-1}\) and a room temperature mobility of 200 000 \(\text{cm}^2\text{V}^{-1}\text{s}^{-1}\). However, the lack of a bandgap also limits the application of graphene. Recently, transition metal dichalcogenides (TMDs), in particular, molybdenum disulfide (MoS2), have attracted a lot of attention. The bulk MoS2 is a semiconductor with an indirect bandgap of \(\sim 1.3\text{eV}\), and the SL MoS2 has a direct bandgap of \(\sim 1.8\text{eV}\). Therefore, MoS2 could complement graphene for many electronic and photonic applications. However, studies of mechanically exfoliated MoS2 on SiO2 found the room temperature mobility is \(<10 \text{cm}^2\text{V}^{-1}\text{s}^{-1}\) for SL-MoS2 and \(10–15 \text{cm}^2\text{V}^{-1}\text{s}^{-1}\) for bilayer MoS2, which are substantially lower than the measured \(\sim 200 \text{cm}^2\text{V}^{-1}\text{s}^{-1}\) of the bulk MoS2 (Ref. 4) or the calculated \(\sim 410 \text{cm}^2\text{V}^{-1}\text{s}^{-1}\) of intrinsic n-type SL-MoS2, which is limited only by optical phonon scattering. The lower than expected mobility is partially due to the long ranged charge disorder or short ranged disorder caused by chemical bonding or roughness at the interfaces. Furthermore, the mechanical exfoliation process cannot be scaled up for practical applications.

Only recently, large-area of SL and few-layer MoS2 films have been synthesized by chemical vapor deposition (CVD).7,8 sulfuration of MoO3,9 or thermolysis of (NH4)MoS4.10 CVD has been demonstrated as the most practical method of synthesizing large-area and high quality graphene,11 boron nitride,12 and boron carbon nitride nanosheets.13 However, devices fabricated from these polycrystalline MoS2 films are still substantially inferior to their exfoliated counterparts.2,14 One possible cause of the degradation of performance is the detrimental effects of the grain boundaries, which can be avoided in the case of graphene by going to a seeded growth single-crystal array approach by CVD to place graphene grains at predetermined locations where devices will be located.15

In this paper, we report the construction of field-effect transistors (FETs) based on single-crystal bilayer and few-layer MoS2 grains. SL, bilayer, and few-layer grains with sizes up to 20 \(\mu\text{m}\) were synthesized directly on SiO2 by CVD. Bilayer and few-layer FETs offer higher on-state current than the SL-MoS2 FET while maintaining high on/off current ratios.3 With a single-crystal bilayer MoS2 conducting channel, we have achieved a superior mobility of 17.3 \(\text{cm}^2\text{V}^{-1}\text{s}^{-1}\) and a current on/off ratio of \(4 \times 10^8\) in a back-gated MoS2 FET.

Our CVD-growth method of single-crystal MoS2 grains is a modification of what is described in Ref. 7 for continuous MoS2 films. However, we do not use seeds as nucleation centers to initiate the growth. Single-crystal MoS2 grains were synthesized in a conventional horizontal quartz tube furnace with sulfur and MoO3 powders as source materials. The MoO3 (0.1 g, Alfa, 99.5%) was placed in an alumina boat and loaded into the center uniform-temperature zone of the furnace. However, we found the residues deposited on the wall of the quartz tube furnace also contribute to the subsequent MoS3 growth, which is not the focus of this paper and will be discussed in detail in another paper.

A piece of Si wafer with 300 nm SiO2 layer was put downstream in a separate boat as substrate. Another alumina boat with 0.4 g sulfur (Alfa, 99.5%) was placed upstream in a low-temperature zone. Before growth, the furnace was evacuated down to \(~70\text{mTorr}\) and back-filled with Ar gas to ambient pressure. In the flow atmosphere of 100 sccm Ar, the furnace was heated to 700°C at the center zone in 60 min subsequently up to 1100°C in 130 min. The temperature of the sulfur and the substrate was increased concurrently to \(~100°C\) and \(~700°C\), respectively. After 20 min, the furnace was cooled down naturally to room temperature.
Raman spectroscopy is used as a non-destructive method to characterize crystalline quality and thickness of MoS2 grains. Representative Raman spectra of SL and bilayer MoS2 grains are shown in Fig. 1(a). For MoS2 crystals, two characteristic Raman active modes, E$_{2g}^1$ and A$_{1g}$, are found. They are associated with the in-plane and out-of-plane vibration of sulfides, respectively. It has been reported that the peak frequency difference between E$_{2g}^1$ and A$_{1g}$ (Δ) can be used to identify the number of MoS2 layers. Figures 2(a) and 2(b) show Raman intensity mappings of E$_{2g}^1$ at 385 cm$^{-1}$ and A$_{1g}$ at 407 cm$^{-1}$ for bilayer; E$_{2g}^1$ at 386 cm$^{-1}$ and A$_{1g}$ at 404 cm$^{-1}$ for single layer. The patterned drain and source metal contact were fabricated on the selected MoS2 grains by electron-beam lithography and a lift-off process.

Photoluminescence spectrum of a typical bilayer MoS2 crystal. The laser excitation wavelength is 532 nm.

Figure 1(b) shows an optical microscopy image of the FET under study. The channel of the FET is bilayer MoS2 determined by Raman spectroscopy. The degenerately doped Si substrate, which is separated from the MoS2 channel by a 300 nm SiO$_2$, is used as a back gate to tune the charge carrier density in the MoS2 channel via the application of a back gate voltage V$_G$. Room temperature electrical measurements were performed under vacuum (10$^{-5}$–10$^{-6}$ Torr) in a Lakeshore TTP6 cryogenic probe station.

Figure 3(b) shows the drain current $I_{DS}$ at fixed drain-source voltage, $V_{DS} = +500$ mV, as a function of the applied back-gate voltage V$_G$, for the device shown in Fig. 3(a). The device is an n-channel normally on FET. The field-effect mobility is determined using the formula: $\mu = (L/W)C_{ox}AG/\Delta V_G$, where $G = I_{DS}/V_{DS}$ is the conductance and $\Delta G / \Delta V_G = (1/V_{DS})(A_{1g}/A_{1g})$ is determined from the slope of a linear-fit of the data with the back-gate voltage ranges from V$_G = +80$ V to V$_G = +100$ V. L = $1 \mu$m is the length and W = $3.6 \mu$m is the width of the MoS2 channel determined from Fig. 3(a). $C_{ox}$ = $\varepsilon_r \varepsilon_0 / d$ is the capacitance per unit area, where d = 300 nm is the thickness of the SiO$_2$ layer with $\varepsilon_0$ = 8.854 × 10$^{-12}$ Fm$^{-1}$ being the free-space permittivity and $\varepsilon_r$ = 3.9 being the relative permittivity of SiO$_2$. The field-effect mobility of the CVD bilayer MoS2 is determined to be 17.3 cm$^2$ V$^{-1}$ s$^{-1}$ comparing to the previously reported 0.02 cm$^2$ V$^{-1}$ s$^{-1}$ of CVD SL-MoS2 (Ref. 7) and 0.04 cm$^2$ V$^{-1}$ s$^{-1}$ of the CVD few-layer MoS2. The much higher mobility of our device may be partially due to the elimination of grain boundary scattering as we reported previously for the CVD graphene. Actually, the 17.3 cm$^2$ V$^{-1}$ s$^{-1}$ mobility of the CVD bilayer MoS2 grain is comparable to the 0.1-10 cm$^2$ V$^{-1}$ s$^{-1}$ reported for exfoliated SL-MoS2 (Ref. 2) and the 10-15 cm$^2$ V$^{-1}$ s$^{-1}$ for exfoliated bilayer MoS2. Another order of magnitude improvement is expected if a high-$\varepsilon$ dielectric is applied on the top of the MoS2 channel to reduce the Coulomb effect.

In Fig. 3(c), the drain current $I_{DS}$ is re-plotted on a logarithmic scale as a function of V$_G$. At V$_G = -100$ V, the
MoS₂ channel of the FET is pinched off with an off-state $I_{DS} < 0.1\,\text{pA}$. The on-state $I_{DS}$ is $> 30\,\mu\text{A}$ with $V_G = +100\,\text{V}$. The corresponding on/off current ratio is $4 \times 10^8$, which is higher than the $\sim 10^4$ on/off current ratio reported for CVD polycrystalline MoS₂ films and comparable to the $\sim 10^9$ of the exfoliated SL-MoS₂ flakes.

Figure 3(d) shows the room temperature transfer characteristics of the FET, i.e., the dependence of drain current on the back-gate voltage at various drain-source voltages. Due to the thick SiO₂ back-gate dielectric, no drain current saturation is observed. For comparison, another back-gated FET with a few-layer (<5 layers) MoS₂ channel was also fabricated, the mobility is also $\sim 17\,\text{cm}^2\text{V}^{-1}\text{s}^{-1}$, while the on/off current ratio might be slightly lower, but still $>10^4$. Most recently, van der Zande et al. also reported the electrical characteristics of CVD single-crystal MoS₂ grains. The mobility measured within a grain was reported to be $3-4\,\text{cm}^2\text{V}^{-1}\text{s}^{-1}$, and the on/off current ratio was in the range of $10^3-10^7$. Our results are consistent with their findings.

It is well known that the best reported mobility of graphene on SiO₂ is limited to $10000\,\text{cm}^2\text{V}^{-1}\text{s}^{-1}$ primarily due to the Coulomb effect. For exfoliated multilayer MoS₂ on SiO₂, the room temperature mobility can be substantially enhanced by engineering the dielectric environment. For example, multilayer MoS₂ has exhibited a mobility $> 100\,\text{cm}^2\text{V}^{-1}\text{s}^{-1}$ when sits on a 50-nm thick atomic layer deposited (ALD) Al₂O₃ (Ref. 14) and $470\,\text{cm}^2\text{V}^{-1}\text{s}^{-1}$ on 50-nm thick spin-coated PMMA. Further enhancement of the MoS₂ mobility can be achieved by applying appropriate gate dielectric on the top of MoS₂ channel. A mobility as high as $\sim 200\,\text{cm}^2\text{V}^{-1}\text{s}^{-1}$ was achieved with a HfO₂/SL-MoS₂/SiO₂ structure, which also exhibits a high on/off ratio ($\sim 10^8$) and low subthreshold swing ($\sim 70\,\text{mV per decade}$).

Thus, in addition to fundamental scientific interests, MoS₂ FETs could be an attractive candidate for low power electronics, e.g., thin-film transistors (TFTs) in the next generation high-resolution liquid crystal (LCD) or organic light-emitting diode (OLED) displays.

In conclusion, we report the electrical characteristics of back gated FETs fabricated on single-crystal MoS₂ grains synthesized by CVD on SiO₂. A FET with a bilayer MoS₂ channel has a mobility $\sim 17\,\text{cm}^2\text{V}^{-1}\text{s}^{-1}$ and an on/off current ratio $\sim 10^8$, while the FET with a few-layer MoS₂ channel exhibits comparable mobility but slightly lower on/off current ratio. Another order of magnitude improvement of mobility is expected by dielectric engineering to reduce the Coulomb effect. The results suggest that CVD is a viable method to synthesize high quality MoS₂ grains with performance comparable to the best mechanically exfoliated MoS₂ flakes, and MoS₂ FETs are promising candidates for low power electronics.

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